REMARKS

Claims 1-36 are pending and are rejected. Claim 16 is amended. Reconsideration and allowance of Claims 1-36 are respectfully requested.

Objections to Drawings

The drawings are objected to. In response thereto, Applicants submit a set of replacement (e.g., formal) drawings in compliance with 37 CFR 1.84, which are attached hereto under separate cover. No new matter is introduced.

Amendments to Specification

Applicants amend paragraph [0065] to correct a clerical error, and amend paragraph [0033] to include updated status information for a referenced U.S. Patent Application. No new matter is introduced.

Claim Amendments

Claim 16 is amended to clarify that which the Applicants regard as the invention. No new matter is introduced.

Claim Rejections under 35 USC §102 over Ohgane

Claims 1-3, 5-9, 12, and 16-36 are rejected under 35 USC §102(b) as being anticipated by Ohgane (USP 5,875,173). Applicants respectfully traverses these rejections.

Independent Claim 1

Applicants' Claim 1 recites:

A traffic management processor for processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit for calculating a departure time for each packet received;

a content addressable memory (CAM) device coupled to the DTC circuit and having a plurality of rows, each row including a first portion for storing the departure

time for a corresponding packet and including a second portion for storing a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow; and

compare logic coupled to the CAM device and configured to determine which of the departure times stored in the CAM device is the earliest.

Ohgane fails to disclose or suggest the traffic management processor of Applicants' Claim 1.

The Office Action equates Ohgane's CAM array 511 with the CAM device recited in Applicants' Claim 1, and then seems to equate Ohgane's collating register 513 with the CBR bits stored in the same CAM device of Applicants' Claim 1 by stating that Ohgane's CAM 511 "includes a second portion for storing a CBR bit (513 of FIG. 4) indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow." Applicants disagree.

First, Ohgane's collating register 513 is NOT part of the CAM 511, but instead is a separate register, as clearly depicted in Figure 4 of Ohgane. Second, Ohgane's collating register 513 stores bits indicating whether corresponding rows of the CAM 511 contain time values that match the counter value provided by the counter 50 during compare operations.[1] Therefore, in contrast to the Examiner's assertion, Ohgane's collating register 513 does NOT store CBR bits indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow, as recited in Applicants' Claim 1, ***but rather stores the match results*** for CAM array 511.[2]

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference[3]. The exclusion of a claimed element from a prior art reference is typically enough to negate anticipation under 35 USC §102. Thus,

---

1 Ohgane states at col. 8, lines 47-52: "the collating register 513 having storage positions corresponding to the respective [CAM] cell array is provided. A logical level "1" is stored in a storage position corresponding to the matched cell array, while a logical level "0" is stored in a storage position corresponding to the unmatched cell array."

2 See also Ohgane at col. 10, lines 21-23, which provides: if agreement between the counter value and the stored value is detected at step S9, a logical "1" representing "agreement" is stored in the collating register 513."

because Ohgane fails to disclose or suggest a traffic management processor including a CAM having a plurality of rows, each row including "a second portion for storing a CBR bit indicating whether the corresponding packet belongs to the UBR traffic flow or to the CBR traffic flow," as recited in Applicants' Claim 1, Claim 1 is patentable over Ohgane. Accordingly, Applicants respectfully request the Office to withdraw the rejection of Claim 1.

Claims 2-15 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

Independent Claim 16

Applicants' Claim 16 (as amended) recites:

A traffic management processor for processing a plurality of packets each having a control bit indicating whether the packet belongs to a traffic flow having an unspecified bit rate (UBR) or belongs to a traffic flow having a constant bit rate (CBR), comprising:

means for generating a departure time for each packet in response to the control bit contained within the packet;

means for queuing the CBR packets and the UBR packets together in the same queue according to their departure times; and

means for selecting the CBR packets and the UBR packets for transmission according to their departure times.

Ohgane fails to disclose or suggest the traffic management processor of Applicants' Claim 16.

The Office Action states that Ohgane discloses a traffic management processor including "means for generating (Line 22-30, Col. 7) a departure time for each packet in response to the control bit (CBR mode and ABR mode, Line 20-24, Col. 6)." Applicants disagree.

The Office Action seems to equate Ohgane's resource management (RM) cell with the control bit recited in Applicants' Claim 16. However, while each packet of

---

3 Corning Glass Works v. Sumitomo Electric, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989).

Claim 16 ***contains*** a control bit that indicates whether the packet belongs to a UBR or a CBR traffic flow, Ohgane's RM cell is a ***separate control cell***, apart from regular data packets, that specifies the peak transmission rate for a virtual channel (VC). For example, Ohgane provides at col. 7, lines 11-19:

> The RM cell detecting section 32 detects from a format of the header whether the received cell is an RM cell or not. If positive, the payload of the received cell is outputted to the transmission time deriving section 34. On the other hand, if the received cell is not the RM cell, the payload of the received cell is stored in the receiving FIFO 33 in sequence. The stored payload is then transferred to the system memory 21 (see FIG. 1) through the DMA operation.

Thus, Ohgane determines whether a received packet is a regular ATM cell or is an RM cell. If the received packet is an RM cell, control information in the RM cell is used to calculate a transmission time for the next ATM cell, and if the received packet is a regular ATM cell, it is output to FIFO for transmission according to the transmission time. Thus, in contrast to Applicants' Claim 16, Ohgane's RM cell updates transmission time information for a ***plurality of other*** ATM cells (e.g., based on peak rates); it is NOT contained in each packet and does NOT indicate whether a corresponding packet belongs to a UBR or CBR traffic flow.

The Office Action also states that Ohgane discloses a traffic management processor including "means for queuing (511 and 513 of FIG. 4) the CBR packets and the UBR packets together according to their departure times (511 of FIG. 4)." Applicants disagree.

There is no language in Ohgane that discloses "queuing the CBR packets and the UBR packets together in the same queue," as recited in Applicants' Claim 16. Instead, Ohgane specifically states that "although explanation has been made to the case where the present invention is applied to the ABR mode, the present invention is also applicable to the CBR mode,"[4] which indicates that Ohgane's description discloses queuing only ABR packets in the queuing mechanism 51, NOT queuing both ABR and CBR packets ***together in the same queue***, as recited in Applicants' Claim 16. Further, Ohgane discusses operating ATM switches in ***either*** a CBR mode ***or*** a

---

4 Ohgane, col. 11, lines 31-34.

UBR mode,[5] which again indicates that Ohgane does not disclose queuing both UBR and CBR traffic together in the same queue, as recited in Applicants' Claim 16.

Accordingly, because Ohgane does not disclose or suggest a traffic management processor that includes "means for generating a departure time for each packet in response to the control bit contained within the packet" and/or "means for queuing the CBR packets and the UBR packets together in the same queue according to their departure times," as recited in Applicants' Claim 16, Claim 16 is patentable over Ohgane.

Claims 16-21 depend from Claim 16 and therefore distinguish over the cited references for at least the same reasons as Claim 16.

Independent Claim 22

Applicants' Claim 22 recites:

A traffic management processor for simultaneously processing an unspecified bit rate (UBR) traffic flow and a constant bit rate (CBR) traffic flow, comprising:

a departure time calculator (DTC) circuit configured to calculate a departure time for each UBR packet and configured to calculate a departure time window for each CBR packet;

a queuing mechanism coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together; and

compare logic coupled to the queuing mechanism and configured to select the packets for departure.

Ohgane fails to disclose or suggest the traffic management processor of Applicants' Claim 22.

The Office Action states that Ohgane discloses a traffic management processor including "a DTC circuit (34 of FIG. 2) configured to calculate (line 22-30, Col. 7) a departure time (transmission time, line 26, Col. 7) for each UBR packet and a departure time window (transmission time, line 26, Col. 7) for each CBR packet." Applicants disagree.

---

5 Ohgane, col. 6, lines 20-27.

The Office Action seems to equate the transmission time calculated in Ohgane with both the departure time for UBR packets and the ***departure window*** for CBR packets recited in Applicants' Claim 22. However, Ohgane discloses calculating only a departure time for packets; Ohgane does NOT disclose or suggest a departure time ***window***, nor has the Office Action pointed to any language in Ohgane that discloses or suggests a "departure time window," as recited in Applicants' Claim 22.

The Office Action also states that Ohgane discloses a traffic management processor including "a queuing mechanism (511 and 513 of FIG. 4) coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together." However, there is no language in Ohgane that discloses "queuing the CBR packets and the UBR packets together," as recited in Applicants' Claim 22. In contrast, Ohgane's description discloses queuing only ABR packets in the queuing mechanism 51, as discussed above with respect to Claim 16, and suggests accommodating both CBR packets and ABR packets by operating in ***either*** a CBR mode ***or*** a UBR mode.[6] Indeed, the Office Action has not pointed to any language in Ohgane that discloses a queuing mechanism "configured to queue the UBR packets and the CBR packets together," as recited in Applicants' Claim 22.

Accordingly, because Ohgane does not disclose or suggest a traffic management processor that includes "a departure time calculator (DTC) circuit configured to calculate a departure time for each UBR packet and configured to calculate a departure time window for each CBR packet" and/or "a queuing mechanism coupled to the DTC circuit and configured to queue the UBR packets and the CBR packets together," as recited in Applicants' Claim 22, Claim 22 is patentable over Ohgane.

Claims 23-27 depend from Claim 22 and therefore distinguish over the cited references for at least the same reasons as Claim 22.

Independent Claim 28

Applicants' Claim 28 recites:

A method of processing a first traffic flow having an unspecified bit rate (UBR)

---

6 Ohgane, col. 6, lines 20-27.

and a second traffic flow having a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for packets belonging to all traffic flows in the same table, each departure time having a CBR bit;

asserting the CBR bit for each packet that belongs to the CBR traffic flow;

de-asserting the CBR bit for each packet that belongs to the UBR traffic flow;

determining which of the departure times that have a de-asserted CBR bit is the earliest; and

transmitting the packet corresponding to the earliest departure time.

Ohgane fails to disclose or suggest method of Applicants' Claim 28.

The Office Action states that Ohgane discloses "storing the departure times (3rd paragraph of Col. 8) for packets belonging to all traffic flows in the same table, each departure time having a CBR bit (513 of FIG. 4)." Applicants disagree.

First, as discussed above with respect to Claim 22, the Office Action has NOT pointed to any language in Ohgane that discloses "queuing the CBR packets and the UBR packets together," and similarly has not pointed to any language in Ohgane that discloses "storing the departure times for packets belonging to all traffic flows in the same table," as recited in Applicants' Claim 28.

Second, the Office Action seems to equate the match signals latched in Ohgane's collating register 513 with the CBR bits recited in Applicants' Claim 28. However, as discussed above with respect to Claim 1, Ohgane's collating register 513 stores match signals indicating whether corresponding rows of the CAM 511 contain time values that match the counter value provided by the counter 50 during compare operations. Therefore, in contrast to the Examiner's assertion, Ohgane's collating register 513 does NOT store CBR bits, ***but rather stores the match results*** for CAM array 511.

Accordingly, because Ohgane does not disclose or suggest a method that includes "storing the departure times for packets belonging to all traffic flows in the same table, each departure time having a CBR bit" and/or "each departure time having a CBR bit," as recited in Applicants' Claim 28, Claim 28 is patentable over Ohgane.

Claims 29-32 depend from Claim 28 and therefore distinguish over the cited references for at least the same reasons as Claim 28.

Independent Claim 33

Applicants' Claim 33 recites:

A method of scheduling packets of traffic flows having either an unspecified bit rate (UBR) or a constant bit rate (CBR), comprising:

calculating a departure time for each packet received;

storing the departure times for the UBR packets and for the CBR packets in a content addressable memory (CAM) device;

comparing the departure times for the UBR packets with each other to determine which departure time is the earliest; and

transmitting the packet corresponding to the earliest departure time.

Ohgane fails to disclose or suggest method of Applicants' Claim 33.

The Office Action states that Ohgane discloses "storing the departure times for the UBR packets and for the CBR packets in a CAM device (511 of FIG. 4)." Applicants disagree.

As discussed above with respect to Claims 16 and 22, the Office Action has NOT pointed to any language in Ohgane that discloses queuing the CBR packets and the UBR packets together, and similarly has not pointed to any language in Ohgane that discloses "storing the departure times for the UBR packets and for the CBR packets in a content addressable memory (CAM) device," as recited in Applicants' Claim 33. In contrast, Ohgane's description discloses queuing only ABR packets in the queuing mechanism 51, and suggests accommodating both CBR packets and ABR packets by operating in ***either*** a CBR mode ***or*** a UBR mode.[7] Thus, while Ohgane discloses storing departure times for ABR packets in CAM array 511, there is no language in Ohgane that discloses storing departure times for ***both CBR and UBR packets*** in the ***same*** CAM device, as recited in Applicants' Claim 33.

7 Ohgane, col. 6, lines 20-27.

Further, the Office Action states that Ohgane discloses "comparing the departure times (511-516 of FIG. 4) for the UBR packets with each other to determine which departure time is the earliest (S9-S12, FIG. 5)." Applicants disagree.

In contrast to the Office Action's assertion, the transmission times (T) stored in Ohgane's CAM array 511 are compared with an input value provided by counter 50;[8] the transmission times are ***not compared with each other***, as recited in Applicants' Claim 33. Indeed, Ohgane further states: "when this time value (T) matches with a value identified by the counter 50, an address where this time value (T) is stored can be determined as a virtual channel VC for the next cell to be transmitted."[9] Thus, Ohgane does NOT disclose or suggest "comparing the departure times for the UBR packets with each other to determine which departure time is the earliest," as recited in Applicants' Claim 33, nor has the Office Action pointed to any such language.

Accordingly, because Ohgane does not disclose or suggest a method that includes "storing the departure times for the UBR packets and for the CBR packets in a content addressable memory (CAM) device" and/or "comparing the departure times for the UBR packets with each other to determine which departure time is the earliest," as recited in Applicants' Claim 33, Claim 33 is patentable over Ohgane.

Claim 34 depends from Claim 33 and therefore distinguishes over the cited references for at least the same reasons as Claim 33.

Independent Claim 35

Applicants' Claim 35 recites:

A method of scheduling packets of traffic flows having either an unspecified bit rate (UBR) or a constant bit rate (CBR), comprising:

calculating a departure time for each UBR packet;

calculating a departure time window for each CBR packet;

queuing the CBR packets and the UBR packets together in the same queuing mechanism; and

---

8 Ohgane states at col. 8, lines 12-15: "When data stored in the CAM cell array section 511 and data inputted as a retrieval pattern are matched or agreed with each other, the CAM 51 outputs an address of the stored data."

9 Ohgane, col. 8, lines 19-22.

selecting the packets for departure according to which packet has the earliest departure time.

Ohgane fails to disclose or suggest method of Applicants' Claim 35.

As discussed above with respect to Claim 22, Ohgane discloses calculating only a departure time for packets; Ohgane does not disclose or suggest a departure time ***window***, nor has the Office Action pointed to any language in Ohgane that discloses or suggests calculating a "departure time window," as recited in Applicants' Claim 35.

Further, as discussed above with respect to Claims 16 and 22, the Office Action has not pointed to any language in Ohgane that discloses queuing the CBR packets and the UBR packets together. In contrast, Ohgane's description discloses queuing only ABR packets in the queuing mechanism 51, and suggests accommodating both CBR packets and ABR packets by operating in ***either*** a CBR mode ***or*** a UBR mode.[10] Indeed, the Office Action has not pointed to any language in Ohgane that discloses "queuing the CBR packets and the UBR packets together in the same queuing mechanism," as recited in Applicants' Claim 35.

Accordingly, because Ohgane does not disclose or suggest "calculating a departure time window for each CBR packet" and/or "queuing the CBR packets and the UBR packets together in the same queuing mechanism," as recited in Applicants' Claim 35, Claim 35 is patentable over Ohgane.

Claim 36 depends from Claim 35 and therefore distinguishes over the cited references for at least the same reasons as Claim 35.

Claim Rejections under 35 USC §103

Claims 4, 10-11, and 13-15 are rejected under 35 USC §103(a) as being unpatentable over Ohgane. Applicants respectfully traverse these rejections.

Claims 4, 10-11, and 13-15 depend from Claim 1 and therefore distinguish over the cited references for at least the same reasons as Claim 1.

---

10 Ohgane, col. 6, lines 20-27.

CONCLUSION

In light of the above remarks, it is believed that Claims 1-36 are in condition for allowance and, therefore, a Notice of Allowance of 1-36 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (408) 236-6646.

Respectfully submitted,

2 April 2007
Dated

William L Paradice III
Attorney for Applicant
Reg. No. 38,990